Amendments to the Claims:

Claims 1, 14 and 15 have been canceled without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously Presented) The system as recited in Claim 21 wherein the target microcontroller is installed on a pod.

3. (Currently Amended) The system as recited in Claim 21 wherein said in circuit emulator base station includes a field programmable gate array (FPGA), and wherein said ~~emulated~~ target microcontroller emulator is programmed into said FPGA.

4. (Previously Presented) The system as recited in Claim 21 wherein the first memory includes a first static random access memory (SRAM) and the second memory includes a second SRAM.

5. (Previously Presented) The system as recited in Claim 21 wherein the first memory includes a first central processing unit (CPU) register and the second memory includes a second CPU register.

6. (Currently Amended) The system as recited in Claim 21 wherein lock step of said microcontroller code execution is maintained by synchronizing said target microcontroller and said ~~emulated~~ target microcontroller emulator.

7. (Previously Presented) The system as recited in Claim 21 wherein said target microcontroller is a production microcontroller.

8. (Previously Presented) The system as recited in Claim 21 wherein said in circuit emulator base station includes a trace buffer.

9. (Currently Amended) A method for debugging microcontroller code comprising:

a) programming said microcontroller code into a target microcontroller including a first memory and into an in circuit emulator base station including a second memory, a trace buffer, and a ~~an emulated~~ target microcontroller emulator which is not identical to and emulates operation of said target microcontroller and initializing said first memory and said second memory;

b) executing the microcontroller code on the target microcontroller and on the ~~emulated~~ target microcontroller emulator in lock step by executing same instructions using same clocking signals;

c) verifying lock step of said executing step by comparing content of the first memory and content of the second memory when said target microcontroller ~~solely on occurrence of any one of said executing step~~ encounters a breakpoint and said executing step halts;

d) if lock step of said executing step is not verified, reporting an error, saving an execution history using said trace buffer and debugging said microcontroller code; and

e) if lock step of said executing step is verified, continuing execution of the microcontroller code.

10. (Previously Presented) The method of Claim 9 further comprising:

locating an error within the microcontroller code by tracing the execution history using the trace buffer.

11. (Previously Presented) The method of Claim 9 wherein said first memory includes a first central processing unit (CPU) register and wherein said second memory includes a second CPU register, wherein said method further comprises:

verifying lock step of said executing step by comparing contents of the first CPU register and contents of the second CPU register.

12. (Currently Amended) The method of Claim 9 wherein said in circuit emulator base station comprises a field programmable gate array (FPGA), and

wherein said ~~emulated~~ target microcontroller emulator is programmed into said FPGA.

13. (Previously Presented) The method of Claim 9 wherein the target microcontroller is a production microcontroller.

14-15. (Canceled)

16. (Previously Presented) The system as recited in Claim 22 wherein the target microcontroller is installed on a pod.

17. (Currently Amended) The system as recited in Claim 22 wherein said in circuit emulator base station includes a field programmable gate array (FPGA), and wherein said ~~emulated~~ target microcontroller emulator is programmed into said FPGA.

18. (Previously Presented) The system as recited in Claim 22 wherein the first memory includes a first central processing unit (CPU) register and the second memory includes a second CPU register.

19. (Previously Presented) The system as recited in Claim 22 wherein said in circuit emulator base station includes a trace buffer.

20. (Previously Presented) The system as recited in Claim 22 wherein the target microcontroller is a production microcontroller.

21. (Currently Amended) A system for debugging microcontroller code, comprising:

a target microcontroller including a first memory;

an in circuit emulator base station including a second memory and a ~~an emulated~~ target microcontroller emulator which is not identical to and emulates operation of said target microcontroller, wherein said target microcontroller and said ~~emulated~~ target microcontroller emulator execute said microcontroller code, wherein said microcontroller code execution occurs in lock step by executing same instructions using same clocking signals; and

an interface coupled to said target microcontroller and said in circuit emulator base station, wherein lock step of said microcontroller code execution is verified by comparing said first memory with said second memory when said target microcontroller ~~solely on occurrence of any one of said microcontroller code execution~~ encounters a breakpoint and said microcontroller code execution halts, and wherein a mismatch between said first and second memories initiates debugging said microcontroller code.

22. (Currently Amended) A system for maintaining lock step execution of microcontroller code during debugging, comprising:

a target microcontroller including a first memory;

an in circuit emulator base station including a second memory and a ~~an emulated~~ target microcontroller emulator which is not identical to and emulates operation of said target microcontroller, wherein said target microcontroller and said ~~emulated~~ target microcontroller emulator execute said microcontroller code, wherein said microcontroller code execution occurs in lock step by executing same instructions using same clocking signals;

a computer system coupled to said in circuit emulator base station and controlling debugging of said microcontroller code; and

an interface coupled to said target microcontroller and said in circuit emulator base station, wherein lock step of said microcontroller code execution is verified by said computer system by comparing said first memory with said second memory when said target microcontroller ~~solely on occurrence of any one of said microcontroller code execution~~ encounters a breakpoint and said microcontroller code execution halts, and wherein a mismatch between said first and second memories initiates debugging said microcontroller code.